Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-60. (canceled)

61. (currently amended) A method comprising:

detecting a transaction that requests access to a memory of a processing system, wherein the processing system comprises a processor that can be set to operate in a normal execution mode in a ring 0 operating mode and, alternatively, to operate in an isolated execution mode in the ring 0 operating mode, wherein the processor also supports one or more higher ring operating modes; and

disallowing the transaction if the transaction requests access to an isolated memory area of the processing system and the processor is not set to operate in the isolated execution mode.

62. (previously presented) A method according to claim 61, wherein:

the operation of disallowing the transaction comprises preventing access to the isolated memory area when the processor is not set to operate in the isolated execution mode; and

the method further comprises allowing access to the isolated memory area when the processor is set to operate in the isolated execution mode.

63. (previously presented) A method according to claim 61, further comprising:

creating the isolated memory area in the memory of the processing system, based at least in part on configuration parameters for defining the isolated memory area.

64. (previously presented) A method according to claim 61, further comprising:

creating the isolated memory area in the memory of the processing system, based at least in part on configuration parameters for the isolated memory area; and

determining whether the transaction requests access to the isolated memory area, based at least in part on access information for the transaction and one or more of the configuration parameters for the isolated memory area.

65. (previously presented) A method according to claim 61, comprising:

determining whether the processor is set to operate in the isolated execution mode, based at least in part on an isolated execution mode setting for the processor.

66. (previously presented) A method according to claim 61, wherein:

the processor comprises a processor control register to store an isolated execution mode setting; and

the method comprises determining whether the processor is set to operate in the isolated execution mode, based at least in part on the isolated execution mode setting from the processor control register.

67. (previously presented) A method according to claim 61, further comprising:

allowing the transaction to succeed if the processor is set to operate in the isolated execution mode.

68. (previously presented) A method according to claim 61, further comprising:

if the processor is set to operate in the isolated execution mode, asserting a signal from the processor to grant access for the transaction.

69. (previously presented) A method according to claim 61, wherein:

the transaction that requests access to the memory of the processing system comprises an access transaction generated during execution of an instruction in the processor.

70. (previously presented) A method according to claim 61, wherein:

the transaction that requests access to the memory of the processing system comprises an access transaction involving one or more resources selected from the group consisting of:

a front side bus (FSB); and

a translation lookaside buffer (TLB).

71. (currently amended) An apparatus comprising:

a processor that can be set to operate in a normal execution mode in a ring 0 operating mode and, alternatively, to operate in an isolated execution mode in the ring 0 operating mode, wherein the processor also supports one or more higher ring operating modes; and

an access checking circuit in the processor, wherein, when the processor is installed in a processing system with memory, the access checking circuit performs operations comprising:

detecting a transaction that requests access to the memory of the processing system; and

disallowing the transaction if the transaction requests access to an isolated memory area of the processing system and the processor is not set to operate in the isolated execution mode.

72. (previously presented) An apparatus according to claim 71, wherein

the operation of disallowing the transaction comprises preventing access to the isolated memory area when the processor is not set to operate in the isolated execution mode; and

the processor allows access to the isolated memory area when the processor is set to operate in the isolated execution mode.

73. (previously presented) An apparatus according to claim 71, wherein the processor performs operations comprising:

creating the isolated memory area in the memory of the processing system, based at least in part on configuration parameters for defining the isolated memory area.

74. (previously presented) An apparatus according to claim 71, wherein the processor performs operations comprising:

creating the isolated memory area in the memory of the processing system, based at least in part on configuration parameters for the isolated memory area; and

determining whether the transaction requests access to the isolated memory area, based at least in part on access information for the transaction and one or more of the configuration parameters for the isolated memory area.

75. (previously presented) An apparatus according to claim 71, wherein the processor performs operations comprising:

determining whether the processor is set to operate in the isolated execution mode, based at least in part on an isolated execution mode setting for the processor.

76. (previously presented) An apparatus according to claim 71, wherein:

the processor comprises a processor control register to store an isolated execution mode setting; and

the processor determines whether the processor is set to operate in the isolated execution mode, based at least in part on the isolated execution mode setting from the processor control register.

77. (previously presented) An apparatus according to claim 71, wherein the processor performs operations comprising:

allowing the transaction to succeed if the processor is set to operate in the isolated execution mode.

78. (previously presented) An apparatus according to claim 71, wherein the processor performs operations comprising:

asserting a signal from the processor to grant access for the transaction if the processor is set to operate in the isolated execution mode.

79. (previously presented) An apparatus according to claim 71, wherein the transaction that requests access to the memory of the processing system comprises an access transaction generated during execution of an instruction in the processor.

80. (previously presented) An apparatus according to claim 71, wherein:

the transaction that requests access to the memory of the processing system comprises an access transaction involving one or more resources selected from the group consisting of:

a front side bus (FSB); and

a translation lookaside buffer (TLB).

81. (currently amended) A processing system comprising:

a processor that can be set to operate in a normal execution mode in a ring 0 operating mode and, alternatively, to operate in an isolated execution mode in the ring 0 operating mode, wherein the processor also supports one or more higher ring operating modes;

memory to include an isolated memory area, the memory responsive to the processor, wherein the memory comprises dynamic random access memory (DRAM); and

an access checking circuit in the processor, wherein the access checking circuit performs operations comprising:

detecting a transaction that requests access to the memory; and

disallowing the transaction if the transaction requests access to the isolated memory area and the processor is not set to operate in the isolated execution mode.

82. (previously presented) A processing system according to claim 81, wherein:

the access checking circuit allows access to the isolated memory area when the processor is set to operate in the isolated execution mode; and

the access checking circuit prevents access to the isolated memory area when the processor is not set to operate in the isolated execution mode.

83. (previously presented) A processing system according to claim 81, wherein the processor performs further operations comprising:

creating the isolated memory area in the memory, based at least in part on configuration parameters for defining the isolated memory area.

84. (previously presented) A processing system according to claim 81, wherein the processor performs further operations comprising:

creating the isolated memory area in the memory, based at least in part on configuration parameters for the isolated memory area; and

determining whether the transaction requests access to the isolated memory area, based at least in part on access information for the transaction and one or more of the configuration parameters for the isolated memory area.

85. (previously presented) A processing system according to claim 81, wherein the processor performs operations comprising:

determining whether the processor is set to operate in the isolated execution mode, based at least in part on an isolated execution mode setting for the processor.

86. (previously presented) A processing system according to claim 81, wherein:

the processor comprises a processor control register to store an isolated execution mode setting; and

the processor determines whether the processor is set to operate in the isolated execution mode, based at least in part on the isolated execution mode setting from the processor control register.

87. (previously presented) A processing system according to claim 81, wherein the processor performs operations comprising:

allowing the transaction to succeed if the processor is set to operate in the isolated execution mode.

88. (previously presented) A processing system according to claim 81, wherein the processor performs operations comprising:

asserting a signal from the processor to grant access for the transaction if the processor is set to operate in the isolated execution mode.

89. (previously presented) A processing system according to claim 81, wherein the transaction that requests access to the memory of the processing system comprises an access transaction generated during execution of an instruction in the processor.

90. (previously presented) A processing system according to claim 81, further comprising:

a front side bus (FSB); and

a translation lookaside buffer (TLB); and

wherein the transaction that requests access to the memory of the processing system comprises an access transaction involving one or more resources selected from the group consisting of:

the FSB; and

the TLB.